

QSFPDD-400G-ER4L-BEW

400GBase QSFP-DD
LWDM4
30km (FEC) Reach

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Features

- QSFP DD MSA compliant
- 400G ER4L specification compliant
- 4 LWDM lanes MUX/DEMUX design
- 8x 26.5625 GBd/s PAM4 electrical interface (400GAUI-8)
- Power dissipation 12W (0~70°C)
- LC duplex connector
- Supports 425 Gb/s aggregate bit rate
- Up to 30 km transmission on single mode fiber with FEC
- Single 3.3 V power supply
- RoHS 2 compliant



Applications

- 400GBASE-ER4L
- Datacenter Interconnect

Part number	Product description
QSFPDD-400G-ER4L-BEW	400GBase SMF QSFP-DD CWDM4 30km 0°C to 70°C LC Duplex DDM (10W)

PIN Description

Pin		Function/Description	Notes
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2-	Transmitter Inverted Data Input	
3	Tx2+	Transmitter Non-Inverted Data output	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4-	Transmitter Inverted Data Input	
6	Tx4+	Transmitter Non-Inverted Data output	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Transmitter Ground (Common with Receiver Ground)	1
14	Rx3+	Receiver Non-Inverted Data Output	
15	Rx3-	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1+	Receiver Non-Inverted Data Output	
18	Rx1-	Receiver Inverted Data Output	
19	GND	Transmitter Ground (Common with Receiver Ground)	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2-	Receiver Inverted Data Output	
22	Rx2+	Receiver Non-Inverted Data Output	
23	GND	Transmitter Ground (Common with Receiver Ground)	1
24	Rx4-	Receiver Inverted Data Output	
25	Rx4+	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMODE	Low Power Mode	
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3+	Transmitter Non-Inverted Data Input	
34	Tx3-	Transmitter Inverted Data Output	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1+	Transmitter Non-Inverted Data Input	
37	Tx1-	Transmitter Inverted Data Output	
38	GND	Transmitter Ground (Common with Receiver Ground)	1

Pin		Function/Description	Notes
39	GND	Transmitter Ground (Common with Receiver Ground)	1
40	Tx6-	Transmitter Inverted Data Input	
41	Tx6+	Transmitter Non-Inverted Data output	
42	GND	Transmitter Ground (Common with Receiver Ground)	1
43	Tx8-	Transmitter Inverted Data Input	
44	Tx8+	Transmitter Non-Inverted Data output	
45	GND	Transmitter Ground (Common with Receiver Ground)	1
46	Reserved	For future use	3
47	VS1	Module Vendor Specific	3
48	VccRx1	3.3V Power Supply Receiver	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Transmitter Ground (Common with Receiver Ground)	1
52	Rx7+	Receiver Non-Inverted Data Output	
53	Rx7-	Receiver Inverted Data Output	
54	GND	Transmitter Ground (Common with Receiver Ground)	1
55	Rx5+	Receiver Non-Inverted Data Output	
56	Rx5-	Receiver Inverted Data Output	
57	GND	Transmitter Ground (Common with Receiver Ground)	1
58	GND	Transmitter Ground (Common with Receiver Ground)	1
59	Rx6-	Receiver Inverted Data Output	
60	Rx6+	Receiver Non-Inverted Data Output	
61	GND	Transmitter Ground (Common with Receiver Ground)	1
62	Rx8-	Receiver Inverted Data Output	
63	Rx8+	Receiver Non-Inverted Data Output	
64	GND	Transmitter Ground (Common with Receiver Ground)	1
65	NC	No Connect	
66	Reserved	For future use	
67	VccTx1	3.3V power supply transmitter	2
68	Vcc2	3.3V power supply	2
69	Reserved	For future use	3
70	GND	Transmitter Ground (Common with Receiver Ground)	1
71	Tx7+	Transmitter Non-Inverted Data Input	
72	Tx7-	Transmitter Inverted Data Output	
73	GND	Transmitter Ground (Common with Receiver Ground)	1
74	Tx5+	Transmitter Non-Inverted Data Input	
75	Tx5-	Transmitter Inverted Data Output	
76	GND	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in the table. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 Ω to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k Ω and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module.

Pin Assignment and Description



Top Side Viewed from Top



Bottom Side Viewed from Bottom

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Ts	-40	85	°C	
Power Supply Voltage	Vcc	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	5	95	%	

Notes:
Exceeding any of these values may be harmful for the device

Recommend Operation Conditions

Parameter	Min	Typ	Max	Unit	Notes
Power Supply Voltage	3.13	3.3	3.47	V	-
Power Supply Current (com.)	-	-	3640	mA	-
Case Operating Temperature (com.)	0	-	+70	°C	-

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Notes
Transmitter					
Differential input Voltage pk-pk	900	-	-	mV	1
Common Mode Voltage	-350	700	2850	mV	2
Single-ended Voltage Tolerance Range	-0.4		3.3	V	-
Differential Input Return Loss	IEEE 802.3-2015 Equation (83E-5)			dB	-
Differential to Common Mode Input Return Loss	IEEE 802.3-2015 Equation (83E-6)			dB	-
Module Stressed Input Test	-	IEEE 802.3cu	-	-	3
Receiver					
Differential output Voltage pk-pk	-	-	900	mV	-
Common Mode Voltage	-350	-	2850	mV	2
Common Mode Noise, RMS	-	-	17.5	mV	-
Transition time	9.5	-	-	ps	4
Near-end Eye height, differential	70	-	-	mV	-
Near-end ESMW (Eye symmetry mask width)	-	0.265	-	UI	-
Far-end ESMW (Eye symmetry mask width)	-	0.2	-	UI	-
Far-end Eye height, differential	30	-	-	mV	-
Far-end pre-cursor ISI ratio	-4.5	-	2.5	%	-
Differential output return loss	IEEE 802.3-2015 Equation (83E-2)				-
Common to differential mode conversion return loss	IEEE 802.3-2015 Equation (83E-3)				-

Notes:

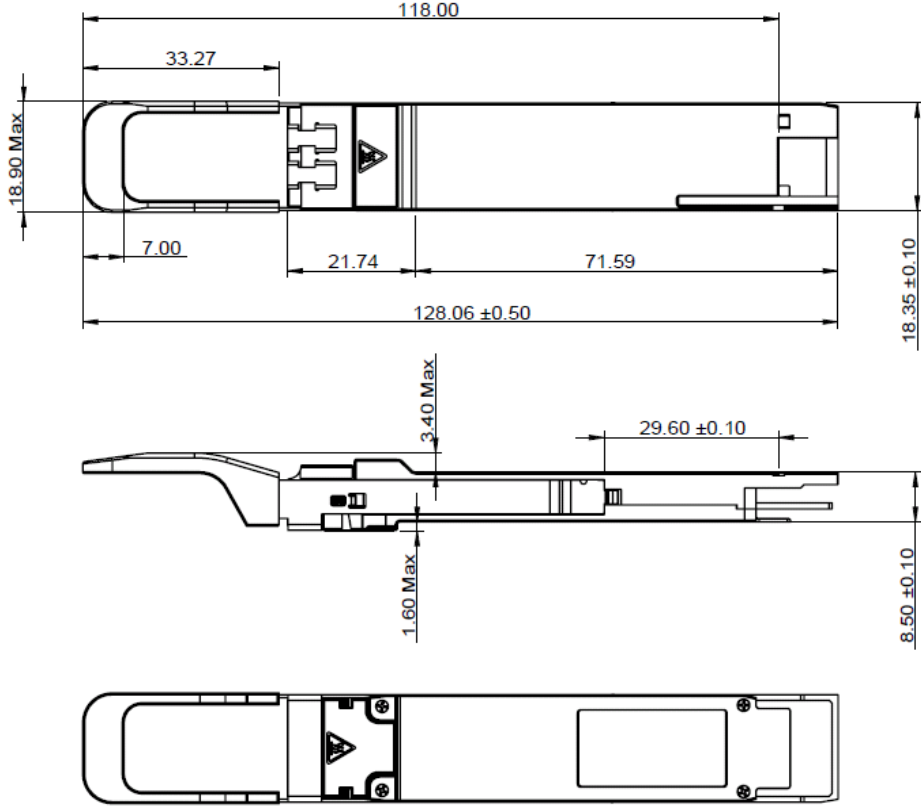
1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
3. BER specified in IEEE 802.3bs 120E.1.1.
4. 20% ~ 80%

Transceiver Optical Characteristics

Parameter	Min	Typical	Max	Units	Notes	
Transmitter						
Average Launch Power per Lane	0.4	-	6.5	dBm	-	
Total Launch Optical Power	-	-	14.7	dBm	-	
Launched Outer OMA(OMA outer) per Lane	3.4	-	6.5	dBm	-	
Difference in Launch Power between any two Lanes (OMA outer)	-	-	4.0	dB	-	
Launched Outer OMA minus TDECQ per Lane	-2.0	-	-	dB	-	
Center Wavelength Range	L0	1294.53	1295.56	1296.59	nm	-
	L1	1299.02	1300.05	1301.09	nm	-
	L2	1303.54	1304.58	1305.63	nm	-
	L3	1308.09	1309.14	1310.19	nm	-
Extinction Ratio per Lane	6.0	-	-	dB	-	
Transmitter and Dispersion Eye Closure (TDECQ) per Lane	-	-	3.9	dB	-	
Data Rate per Lane	-	53.125	-	GBd/s	-	
Receiver						
Center Wavelength Range	L0	1294.53	1295.56	1296.59	nm	-
	L1	1299.02	1300.05	1301.09	nm	-
	L2	1303.54	1304.58	1305.63	nm	-
	L3	1308.09	1309.14	1310.19	nm	-
Damage Threshold per Lane	-3.4	-	-	dBm	-	
Sensitivity per Lane	-	-	-12.1, SECQ-13.5	dBm	-	
Stressed Eye Closure for PAM4 (SECQ), Lane under Test	-	3.4	-	dBm	-	
OMAouter of each Aggressor Lane	-	-8.0	-	dBm	-	



Mechanical specifications



Revision history

Revision	Date	Author	Description
V1.1	31-04-2022	JGN	Initial Document

Note : Nexgen A/S reserves the right to change this document without notice.