QSFPDD-400G-PDAC-xM

400GBase QSFP-DD to QSFP-DD
Passive Copper Cable
Up to 3m Reach

Datasheet | product specifications

ESD threshold 1kV for SFI pins and 2kV for all other electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114A (HBM). However, normal ESD precautions are still required during the handling of this module.

Features

- Compatible with IEEE 802.3bj and IEEE 802.3cd
- Supports aggregate data rates of 400Gbps (PAM4)
- Up to 3m reach
- Pull-to-release slide latch design
- 28AWG through 30AWG cable
- Straight and break out assembly configurations available
- Customized cable braid termination limits EMI radiation
- Lowest total system power solution
- RoHS compliant

Applications

- Switches,servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment

Overview

Part Number	Data Rate	Cable Jacket	Cable Length	AWG	Temperature
QSFPDD-400G-PDAC-0.5M	400Gbps	PVC	0,5m	30	0°C to 70°C
QSFPDD-400G-PDAC-1M	400Gbps	PVC	1m	30	0°C to 70°C
QSFPDD-400G-PDAC-1.5M	400Gbps	PVC	1.5m	30	0°C to 70°C
QSFPDD-400G-PDAC-2M	400Gbps	PVC	2m	28	0°C to 70°C
QSFPDD-400G-PDAC-2.5M	400Gbps	PVC	2.5m	28	0°C to 70°C
QSFPDD-400G-PDAC-xM	400Gbps	PVC	3m	28	0°C to 70°C

Ordering Information

Part number	Product description
QSFPDD-400G-PDAC-xM	400GBase QSFP-DD to QSFP-DD Passive DAC xm, x= value for meters (e.g. 3M = 3 meters length)

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PIN Description

PIN	Symbol	Name - Description	Logic	Notes
1	GND	Ground		1
2	Tx2n	Transmitter Inverted Data Input	CML-I	
3	Tx2p	Transmitter Non-Inverted Data Input	CML-I	
4	GND	Ground		1
5	Tx4n	Transmitter Inverted Data Input	CML-I	
6	Tx4p	Transmitter Non-Inverted Data Input	CML-I	
7	GND	Ground		1
8	ModSelL	Module Select	LVTTL-I	
9	ResetL	Module Reset	LVTTL-I	
10	VccRx	+3.3V Power Supply Receiver		2
11	SCL	2-Wire serial Interface Clock	LVCOMS-I/O	
12	SDA	2-Wire serial Interface Data	LVCOMS-I/O	
13	GND	Ground		1
14	Rx3p	Receiver Non-Inverted Data Output	CML-O	
15	Rx3n	Receiver Inverted Data Output	CML-O	
16	GND	Ground		1
17	Rx1p	Receiver Non-Inverted Data Output	CML-O	
18	Rx1n	Receiver Inverted Data Output	CML-O	
19	GND	Ground		1
20	GND	Ground		1
21	Rx2n	Receiver Inverted Data Output	CML-O	
22	Rx2p	Receiver Non-Inverted Data Output	CML-O	
23	GND	Ground		1
24	Rx4n	Receiver Inverted Data Output	CML-O	
25	Rx4p	Receiver Non-Inverted Data Output	CML-O	
26	GND	Ground		1
27	ModPrsL	Module Present	LVTTL-O	
28	IntL/RxLOS	Interrupt/optional RxLOS	LVTTL-O	
29	VccTx	+3.3V Power supply transmitter		2
30	Vcc1	+3.3V Power supply		2
31	LPMode	Low Power mode	LVTTL-I	
32	GND	Ground		1
33	Tx3p	Transmitter Non-Inverted Data Input	CML-I	
34	Tx3n	Transmitter Inverted Data Input	CML-I	
35	GND	Ground		1
36	Tx1p	Transmitter Non-Inverted Data Input	CML-I	
37	Tx1n	Transmitter Inverted Data Input	CML-I	
38	GND	Ground		1
39	GND	Ground		1
40	Tx6n	Transmitter Inverted Data Input	CML-I	
41	Tx6p	Transmitter Non-Inverted Data Input	CML-I	
42	GND	Ground		1

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PIN	Symbol	Name - Description	Logic	Notes
43	Tx8n	Transmitter Inverted Data Input	CML-I	
44	Tx8p	Transmitter Non-Inverted Data Input	CML-I	
45	GND	Ground		1
PIN	Symbol	Name - Description	Logic	Notes
46	Reserved	For Future Use	LVCMOS/CML-I	3
47	P/VS1	Programmable/Module Vendor Specific 1	LVCMOS/CML-I	3
48	VccRx1	+3.3V Power Supply		2
49	P/VS2	Programmable/Module Vendor Specific 2	LVCMOS/CML-O	3
50	P/VS3	Programmable/Module Vendor Specific 3	LVCMOS/CML-O	3
51	GND	Ground		1
52	Rx7p	Receiver Non-Inverted Data Output	CML-O	
53	Rx7n	Receiver Inverted Data Output	CML-O	
54	GND	Ground		1
55	Rx5p	Receiver Non-Inverted Data Output	CML-O	
56	Rx5n	Receiver Inverted Data Output	CML-O	
57	GND	Ground		1
58	GND	Ground		1
59	Rx6n	Receiver Inverted Data Output	CML-O	
60	Rx6p	Receiver Non-Inverted Data Output	CML-O	
61	GND	Ground		1
62	Rx8n	Receiver Inverted Data Output	CML-O	
63	Rx8p	Receiver Non-Inverted Data Output	CML-O	
64	GND	Ground		1
65	NC	No Connect		3
66	Reserved	For future use		3
67	VccTx1	+3.3 V Power Supply		2
68	Vcc2	+3.3 V Power Supply		2
69	ePPS/Clock	1PPS PTP clock or reference clock input	LVCMOS-I	4
70	GND	Ground		1
71	Tx7p	Transmitter Non-Inverted Data Input	CML-I	

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500mA.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connect ed within the module in any combination. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1000mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50Ω to ground on the host. Pad 65 (No Connect) shall be left uncon nected within the module, optionally pad 65 may get terminated with 10kΩ to ground on the host. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10kΩ.

4. For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

Pin Assignment and Description

Top Side Viewed from Top

Bottom Side Viewed from Bottom

Recommended Operating Conditions

Parameters	Symbols	Min	Typ	Max	Unit	Notes
Differential Impedance	TDR	90	100	110	Ω	
Insertion Loss	SDD21	-16.06			dB	@ 13.28 GHz
Differential Return Loss	SDD11 SDD22			Note 1 Note 2	dB	[0.05 ; 4.1] GHz [4.1 ; 19] GHz
Common-mode to commonmode output return loss	SCC11 SCC22			-2 -2	dB	[0.20 ; 19] GHz [0.20 ; 19] GHz
Differential to common-mode return loss	SCD11 SCD22			Note 3 Note4	dB	[0.01 ; 12.89] GHz [12.89 ; 19] GHz
Differential to common-mode conversion loss	SCD21 IL			-10 Note 5 -6.3	dB	[0.01 ; 12.89] GHz [12.89 ; 15.7] GHz [15.7 ; 19] GHz

Notes:
1. Reflection Coefficient given by equation SDD11(dB) < -16.5 + 2 × SQRT(f), with f in GHz
2. Reflection Coefficient given by equation SDD11(dB) < -10.66 + 14 × log10(f/5.5), with f in GHz
3. Reflection Coefficient given by equation SCD11(dB) < -22 + (20/25.78)*f, with f in GHz
4. Reflection Coefficient given by equation SCD11(dB) < -15 + (6/25.78)*f, with f in GHz
5. Reflection Coefficient given by equation SCD21(dB) < -27 + (29/22)*f, with f in GHz

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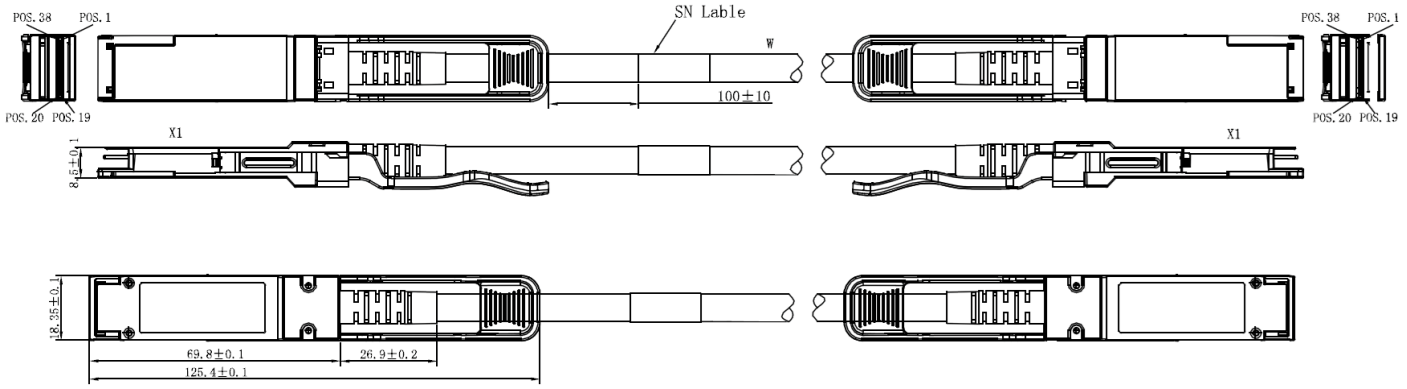
Cable AWG Type

Cable Length	Cable AWG
0.5	30
1	30
1.5	30
2	28
2.5	28
3	28

Block Diagram



Revision History

Revision	Doc. #	Date	Author	Description
Version 1.1	DT000233	06/02/2026	GS	Updated Document

Note: Nexgen A/S reserves the right to change this document without notice.